TITLE OF THE INVENTION

ERROR CORRECTION METHOD AND APPARATUS FOR LOW DENSITY PARITY CHECK

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of PCT International Patent Application No. PCT/KR2004/003079, filed November 26, 2004, and Korean Patent Application No. 2003-85769, filed November 28, 2003 in the Korean Intellectual Property Office, the disclosures of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] Aspects of the present invention relate to an error correction method and apparatus, and more particularly, to a method of and an apparatus for determining whether an error exists in a decoded binary signal and correcting the error if the error exists in a decoding apparatus using a low density parity check (LDPC).

2. Description of the Related Art

[0003] A low density parity check (LDPC) encoding and decoding method refers to an error correction encoding and decoding technology used in a wireless communication field and an optical recording/reproducing field. An LDPC encoding includes a process of generating parity information using a parity check matrix. Here, most components of the parity check are 0, and very sparse components of the parity check matrix are 1.

[0004] The LDPC encoding may be divided into a regular LDPC encoding and an irregular LDPC encoding. In the regular LDPC encoding, the number of components equal to 1 included in a parity check matrix used for encoding and decoding is the same in every row and column. Otherwise, the LDPC encoding is irregular.

[0005] The LDPC encoding can be represented as shown in Equation 1.

$$H \times C_e = 0 \qquad \ldots(1)$$

where, H indicates a parity check matrix, 0 indicates a zero matrix, 'x' indicates an exclusive OR

(XOR) operation and a modular 2 operation, and C_e indicates a code word vector, that is, a column matrix indicating a code word to be encoded. The code word includes an x-bit message word $x_1, x_2,\ldots, x_x$ and p-bit parity information $p_1, p_2,\ldots, p_p$.

[0006] The parity information $p_1, p_2,\ldots, p_p$ is generated so that the message word $x_1, x_2,\ldots, x_x$ satisfies Equation 1. That is, since a binary value of the message word to be encoded among components of the parity check matrix H and matrix C is determined, parity information p_i (i = 1, 2,..., p) can be determined using Equation 1.

[0007] The LDPC decoding can be represented as shown in Equation 2.

$$H \times C_d = Z \qquad \ldots(2)$$

where, H indicates the same parity check matrix as that used for the encoding, C_d indicates a code word vector after passing a channel, and Z indicates a resultant matrix generated by performing a modular 2 operation on the H and C_d matrices. If an original code word is restored by successfully performing the decoding, that is, if $C_e = C_d$, the resultant matrix will be the zero matrix. That is, it is determined whether the decoding is successful by determining whether all components of the resultant matrix Z are 0.

[0008] More detailed descriptions of the LDPC encoding are described in "Good Error Correction Codes Based on Very Sparse Matrices" (D.J. MacKay, IEEE Trans. On Information Theory, vol. 45, no. 2, pp 399-431, 1999) and "Efficient Encoding of Low Density Parity Check Codes" (T. Richardson, R. Urbanke, IEEE Trans. On Information Theory, vol. 47, no. 2, pp 638-656, 2001).

[0009] However, according to the conventional LDPC decoding method described above, since the resultant matrix Z cannot be equal to the zero matrix even if an error is generated in only one bit of the decoded word vector C_d, the decoding is determined as a failure. Therefore, the conventional LDPC decoding method is not an efficient decoding method.

SUMMARY OF THE INVENTION

[0010] Aspects of the present invention provide a low density parity check (LDPC) error correction method and apparatus for preventing a small number of errors from causing a total

block to be determined as a decoding failure and correcting an error when it is determined that the error is in only one bit.

[0011] According to aspects of the LDPC decoding method and apparatus of embodiments of the present invention, the decoding apparatus using the LDPC can prevent a small number of errors from causing a total block to be determined as a decoding failure and correct an error when it is determined that a 1-bit error exists.

[0012] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a flowchart of an LDPC error correction method according to an embodiment of the present invention;

FIG. 2 is a block diagram of an error correction apparatus according to an embodiment of the present invention;

FIG. 3 illustrates correlations among components of matrices in a regular LDPC decoding;

FIG. 4 illustrates an example of correlations among components of matrices representing a principle of an error determination and correction method according to an embodiment of the present invention; and

FIG. 5 is a flowchart of an error determination and correction method according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0014] According to an aspect of the present invention, a low density parity check (LDPC) error correction method comprises: generating a resultant matrix (m*1) by performing an exclusive OR (XOR) operation and a modular 2 operation with respect to an LDPC matrix (m*n)

and a code word vector (n*1); determining whether a decoding of the code word vector succeeded based on the resultant matrix; and if it is determined that the decoding failed, detecting a code word bit, in which an error is generated, in the code word vector based on correlations of components of the LDPC matrix, the code word vector, and the resultant matrix.

[0015] According to another aspect of the present invention, an error determination method comprises: generating a resultant matrix (m*1) by multiplying an LDPC matrix (m*n) by a code word vector (n*1) and determining whether a decoding of the code word vector succeeded based on the resultant matrix; and if it is determined that the decoding failed, determining again whether the decoding succeeded based on a number of 1s included in the resultant matrix.

[0016] According to another aspect of the present invention, a low density parity check (LDPC) error correction apparatus comprises: a decoding success/failure checking unit generating a resultant matrix (m*1) by performing an XOR operation and a modular 2 operation with respect to an LDPC matrix (m*n) and a code word vector (n*1) and determining whether a decoding of the code word vector succeeded based on the resultant matrix; an error location detector searching a same column vector as the resultant matrix in the LDPC matrix and, if the same column vector exists, detecting an error location by detecting a column number of the same column vector.

[0017] Reference will now be made in detail to the present embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0018] FIG. 1 is a flowchart of an LDPC error correction method according to an embodiment of the present invention.

[0019] A decoding success/failure check of a decoded code word vector is performed in operation 100. This operation is performed by determining whether all components of a resultant matrix Z obtained by performing an XOR operation and a modular 2 operation of a parity check matrix H and decoded code word vector C are 0 in accordance with Equation 2.

[0020] If it is determined that the decoding failed in operation 100, that is, if even a single '1' is discovered in the resultant matrix Z, it is determined whether the generated error is a 1-bit error in operation 110. A first condition of the 1-bit error is that a number of 1s generated in the resultant matrix Z is the same as a number of 1s included in a column of the parity check matrix H. That is, the first condition of 1-bit error is related to the number of errors. The reason is because a change of a code word bit influences generation of the resultant matrix Z as much as the number of 1s included in a specific column of the parity check matrix H. As a result, if the number of 1s included in the resultant matrix Z is not the same as the number of 1s included in a column of the parity check matrix H, it is determined that the error is not the 1-bit error.

[0021] If it is determined that the error is not the 1-bit error in operation 110, a decoder (not shown) determines that the decoding failed and finished the decoding process at the moment. However, if it is determined that the error is the 1-bit error in operation 110, it is determined whether the decoded code word vector C satisfies a second condition to be the 1-bit error in operation 120. The second condition to be the 1-bit error is that the same column vector as the resultant matrix Z must exist in the parity check matrix H. That is, the second condition to be the 1-bit error is related to an error location. The second condition will be described in detail with reference to FIGS. 3 and 4.

[0022] If the two conditions to be the 1-bit error are satisfied in operations 110 and 120, a 1-bit error correction is performed in operation 130. The 1-bit error correction is performed by changing binary values of code word bits corresponding to a column number of the column vector detected in operation 120 in the code word vector.

[0023] FIG. 2 is a block diagram of an error correction apparatus according to an embodiment of the present invention.

[0024] Referring to FIG. 2, the error correction apparatus includes a decoding success/failure checking unit 210, an error count detector 220, an error location detector 230, and a binary value changing unit 240. The decoding success/failure checking unit 210 determines whether a decoding succeeded or failed by generating a resultant matrix Z (221) from a code word vector C (211), which is decoded binary signal, and a parity check matrix, and determining whether all components of the resultant matrix Z (221) are 0.

[0025] If it is determined that the decoding failed, the error count detector 220 receives the resultant matrix Z (221), detects a number of 1s included in the resultant matrix Z (221), and determines whether the number of detected 1s is the same as a column weight of the parity check matrix H. If the number of detected 1s and the column weight of the parity check matrix H are the same, the error count detector 220 generates a first condition satisfaction signal 231 and transmits the signal 231 to the error location detector 230. When the error location detector 230 receives the first condition satisfaction signal 231 from the error count detector 220, the error location detector 230 searches whether the same column vector as the resultant matrix Z (221) exists in the parity check matrix H. If the same column vector exists, the error location detector 230 transmits a second condition satisfaction signal 241 and a column number k of the detected column vector to the binary value changing unit 240.

[0026] When the binary value changing unit 240 receives the second condition satisfaction signal 241 from the error location detector 230, the binary value changing unit 240 corrects the error by changing a binary value of a code word bit, which has the same number as the column number k of the column vector received from the error location detector 230, in the code word vector C (211).

[0027] FIG. 3 illustrates correlations among components of matrices in a regular LDPC decoding.

[0028] An LDPC matrix H is an m*n matrix having components h_{11} through h_{mn}. In a regular LDPC encoding, a same number of 1s is included in each row R_1, R_2, R_3,..., R_n, and a same number of 1s included in each column C_1, C_2, C_3,..., C_n. The number of 1s in each row R_1, R_2, R_3,..., R_n is called a row weight, and the number of 1s included in each column C_1, C_2, C_3,..., C_n is called a column weight. In a typical regular LDPC encoding, the row weight is 3, and the column weight is usually 9, which is three times the row weight.

[0029] In a regular LDPC decoding, each row R_1, R_2, R_3,..., R_n is different from each other row, and each column C_1, C_2, C_3,..., C_n is also different from each other column. That is, R_1, R_2, R_3,..., R_n, are respectively different and C_1, C_2, C_3,..., C_n are respectively different. This feature is used for an error correction that is described below.

[0030] A decoded word vector C includes code word bits x_1, x_2, x_3,..., x_n including information

bit and parity bit. The resultant matrix Z is generated by performing a modular operation of the LDPC matrix H and decoded word vector C.

[0031] Correlations among components of the matrices are represented as shown in Equations 3.

$$\left.\begin{aligned} &\text{mod } 2[h_{11}x_1 + h_{12}x_2 + \ldots + h_{1n}x_n] = z_1 \\ &\text{mod } 2[h_{21}x_1 + h_{22}x_2 + \ldots + h_{2n}x_n] = z_2 \\ &\ldots \\ &\text{mod } 2[h_{m1}x_1 + h_{m2}x_2 + \ldots + h_{mn}x_n] = z_m \end{aligned}\right\} \quad \ldots(3)$$

Here, if any one of $z_1, z_2, z_3, \ldots, z_n$ is 1, it is determined that the decoding failed.

[0032] FIG. 4 illustrates correlations among components of matrices representing a principle of an error determination and correction method according to an embodiment of the present invention.

[0033] Referring to FIG. 4, a column weight (CW) is 3, and a parity check matrix H is a 10*20 matrix. Code word bits $x_1, x_2, x_3, \ldots, x_{20}$ indicates decoded code word bits. A resultant matrix Z is a column vector having 10 components.

[0034] In the example shown in FIG. 4, third, seventh, and tenth components of the resultant matrix Z are 1. This resultant matrix Z indicates that the LDPC decoding failed. Now, it is determined which component of the resultant matrix Z is generated from which components of the parity check matrix H and decoded code word vector C and which components give which kind of influences to the error. The above determinations can be made by examining Equation 3.

[0035] A first '1' (411) of the resultant matrix Z is generated by performing the modular operation of a third row R3 of the parity check matrix H and the code word column vector. A second '1' (412) of the resultant matrix Z is generated by performing the modular operation of a seventh row R7 of the parity check matrix H and the code word column vector. Likewise, a third '1' (413) of the resultant matrix Z is generated by performing the modular operation of a tenth row R10 of the parity check matrix H and the code word column vector. If the decoded code word vector C were to be the same as a code word vector C, no '1' would appear in the

resultant matrix Z. However, since at least one '1' appears in the resultant matrix Z, it can be predicted that binary values of one or more (unknown yet) bits among code word bits of the decoded code word vector C were changed. In the embodiment of the present invention, when only one code word bit is changed, that is, when a 1-bit error is generated, a location where the error is generated is predicted.

[0036] In the example shown in FIG. 4, it is assumed that an error is generated in one bit of the decoded code word vector C and a location where the error is generated is a tenth code word bit x_{10} of the decoded code word vector C. In Equation 3, when the resultant matrix Z is generated, the code word bit x_{10} is modular 2 operated with each bit of a tenth column C_{10} of the parity check matrix H. However, the code word bit x_{10} is not modular 2 operated with all bits of the tenth column C_{10} since there are components having a value 0. That is, the code word bit x_{10} is modular 2 operated in only locations where '1' exists among components of the tenth column C_{10}, and as a result only the locations influence the generation of components of the resultant matrix Z. In the example shown in FIG. 4, since the locations where a component of the tenth column C_{10} is 1 are the third, seventh, and tenth bits, 1s appear in the third, seventh, and tenth locations of the resultant matrix Z.

[0037] As a result, if only a 1-bit error is generated, it can be known that column numbers of the parity check matrix H having '1' in the same locations as those where '1' appears in the resultant matrix Z are the same as numbers of code word bits where errors are generated in the decoded code word vector C. However, this proposition assumes that the parity check matrix H is a regular LDPC matrix and an error is generated in only one bit of the code word. If the error is not the 1-bit error, since a plurality of code words influence generation of components of the resultant matrix, and since a row of the parity check matrix and the generation of components of the resultant matrix do not have a one-to-one relationship, the code word bits which influence the generation of the resultant matrix are unknown.

[0038] As described above, a bit where an error is generated in the code word can be determined by examining the resultant matrix, as follows.

[0039] First, bit numbers whose values are 1 in the resultant matrix are detected. In the example shown in FIG. 4, the bit numbers whose components have 1 in the resultant matrix are 3, 7, and 10, references (411), (412) and (413), respectively.

[0040] Second, the parity check matrix H is searched for a column C_k having 1 bits in a same location as 1 bits detected in the resultant matrix. In a regular LDPC, since every column of the parity check matrix is different, the column C_k having 1 bits in the same location as the resultant matrix is unique. In the example shown in FIG. 4, the column C_k is C_{10}, and the corresponding 1 bits are identified by references (401), (402) and (403), respectively.

[0041] Third, a code word bit having a same number as the number of the column C_k having 1 bits which match the 1 bits of the resultant matrix is determined to be the code word bit where the error is generated. In the example shown in FIG. 4, the code word bit having the error is determined to be x_{10}.

[0042] As described above, it is assumed that a 1-bit error is generated and every column of a parity check matrix has the same column weight. Therefore, if the number of bits having 1 in the resultant matrix is not the same as the column weight (for example, the number of bits having 1 in the resultant matrix is 4), an error bit is not determined.

[0043] An LDPC matrix used for optical disc systems usually uses cases where m = 1000 through 10000 and n = 3000 through 30000. If it is considered that a general bit error rate (BER) of a DVD is 10^{-12}, a proportion of generating errors in two bits or more with respect to one code word vector (3000 through 30000 bits) is very low. Therefore, in general optical disc systems, a very large error correction effect can be achieved with only a 1-bit error correction.

[0044] FIG. 5 is a flowchart of a method of error determination and correction according to an embodiment of the present invention.

[0045] Operations 510 and 520 detect whether an error exists in an encoded code word vector C. The decoding success/failure checking unit 210 generates a resultant matrix Z by multiplying a parity check matrix H used in an encoding process and a decoded code word vector C and performing a modular 2 operation on respective components of the two matrices in operation 510. The decoding success/failure checking unit 210 checks whether all components of the resultant matrix Z are 0 in operation 520. Since the modular 2 operation was performed, if an error was not generated in the decoded code word vector C, all components of the resultant matrix Z should be 0. However, if at least one '1' exists in the components of the resultant matrix Z due to error generation, the method proceeds to operation 530.

[0046] Operations 530 and 540 indicate a first procedure determining whether the error generated in the decoded code word vector C is a correctable error according to the embodiment of the present invention, that is, whether the error is a 1-bit error. If it is determined that at least one '1' is included in the components of the resultant matrix Z in operation 520, the error count detector 220 detects the number of 1s included in the resultant matrix Z in operation 530 and determines whether the number of 1s is included in the decoded code word vector C is the same as a column weight (CW) of the parity check matrix in operation 540. if the number of 1s included in the decoded code word vector C is different from the CW of the parity check matrix H in operation 540, since the error is not the 1-bit error, the error cannot be corrected according to the embodiment of the present invention. Accordingly, it is determined that the decoding failed. If the number of 1s included in the decoded code word vector C is the same as the CW of the parity check matrix H in operation 540, the method proceeds to operation 550.

[0047] Operations 550 through 570 indicate a second procedure determining whether the error generated in the decoded code word vector C is a correctable error according to the embodiment of the present invention, that is, whether the error is a 1-bit error. If it is determined that the number of 1s included in the decoded code word vector C is the CW of the parity check matrix H in operation 540, the error location detector 230 compares each column matrix C_1, C_2, C_3,..., C_n included in the parity check matrix H to the resultant matrix Z in operation 550 and determines whether a column matrix C_k is the same as the resultant matrix Z exists in operation 560. If it is determined that a column matrix C_k which is the same as the resultant matrix Z does not exist in operation 560, the error cannot be corrected according to the embodiment of the present invention, since the error is not the 1 bit error. Accordingly it is determined that the decoding failed. If the column matrix C_k, which is the same as the resultant matrix Z exists in operation 560, a column number k of the column matrix C_k is extracted in operation 570.

[0048] The binary value changing unit 240 generates a corrected code word vector C' by changing a binary value of the k^{th} code word bit of the decoded code word vector C, that is, changing 0 to 1 or 1 to 0, in operation 580. Since every codeword bit has only a value of 0 or 1, if the error is generated on a value 0, 1 is a value before the error is generated. Accordingly, the binary value changing allows the error to be corrected.

[0049] In operations 590 and 600, the decoding success/failure checking unit 210 confirms whether the correction is achieved by checking the corrected code word vector C' using a same procedure as operations 510 and 520.

[0050] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in this embodiment without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.